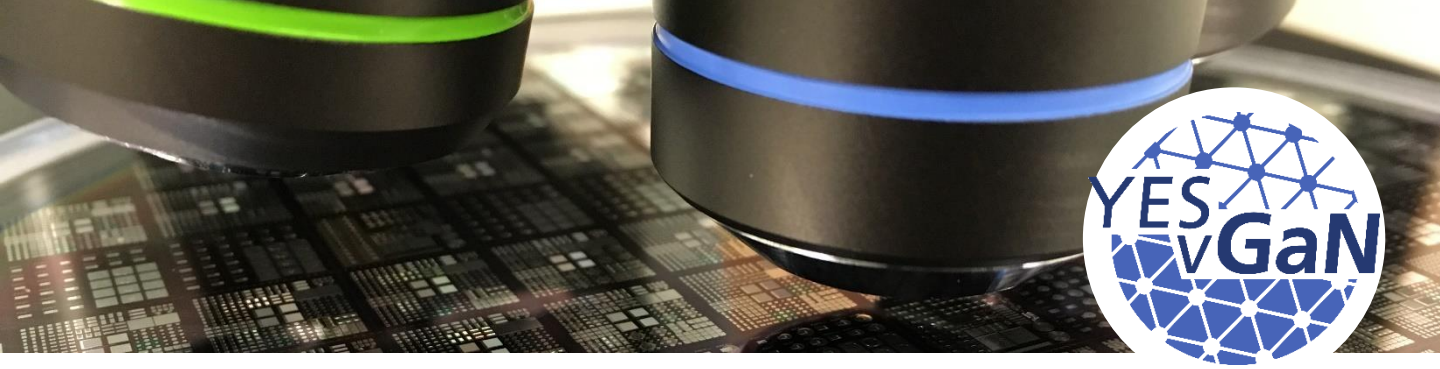

YESvGaN

Wide bandgap power at silicon cost

Newsletter 2 – April 2023

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Introduction

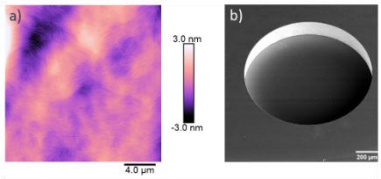
The second year in the YESvGaN journey of developing vertical GaN membrane transistors has come to its end. Our vision is to establish a new class of power transistors which can combine the performance benefits of vertical wide band gap power transistors with the cost benefits of heteroepitaxial growth of GaN on foreign substrates. The consortium of 23 European partner has continued to show strong dedication in order to make affordable and efficient vertical GaN technology a reality. As the development of thick hetero-epitaxial layers was intensified, previously developed process modules were merged to full front and backside process flows and the first electrically active diode chips could be assembled. We are very pleased to provide a short overview of the recent technology highlights in this newsletter.

Development of vertical drift epitaxy

The development of industrial equipment is an essential part of the YESvGaN project. This year, we successfully built and tested a prototype 300 mm MOCVD system with automated cassette-to-cassette hand-ling in the AIXTRON laboratory.

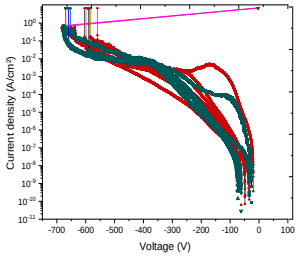
Pictures of the 300 mm MOCVD system with EFEM module.

Apart from MOCVD we also investigated an alternative GaN epi technique via regrowth from nanowire-templates, resulting in smooth surfaces with a rms roughness of 0.15 nm.

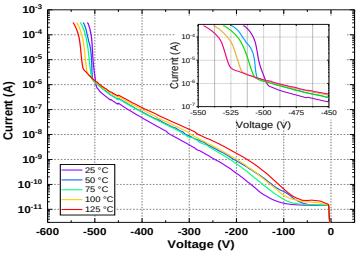


AFM images (left) and SEM image (right) of a membrane structure grown via nanowire-templates.

We reached a milestone this year by growing vertical drift layer stacks on Si with a breakdown voltage of 650V! On sapphire vertical drift layer stacks, we showed avalanche breakdown behavior, confirming the high crystal quality of the GaN.



Reverse I-V curves of pn-diodes on Si



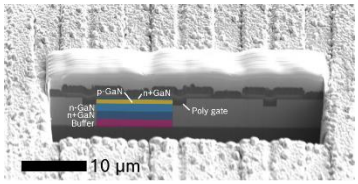
Reverse I-V curves of pn-diodes on Sapphire

Material characterization continued, with additional efforts to investigate GaN membranes where the substrate has been removed. Characterization by AFM, SEM, KPFM and Raman, confirmed the fabrication of healthy membranes.

Development of vertical GaN power transistors

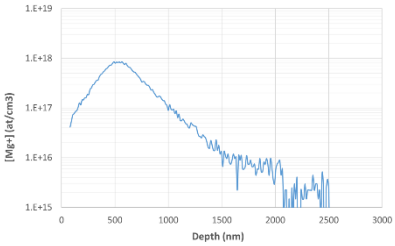
This year, we fabricated pseudo-vertical trench gate MOSFETs showing normally-off behavior with a channel mobility of 17 cm^2/Vs on GaN-on-Si with a gate first process, improving compatibility with standard Si fabs. For vertical GaN FinFETs, we demonstrated the advantage of mixing plasma enhanced and thermal ALD for the gate dielectric with a detailed study using in vacuo XPS and electrical measurements.

Pseudo-vertical trench gate MOSFET



Recently, we rolled the first 200mm GaN-on-Si wafers with their frontside fully processed out of the production line. We believe this is an important demonstration that vertical GaN-on-Si is feasible in an industrialized environment.

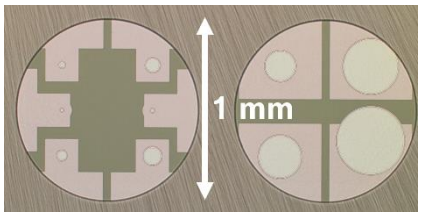
SIMS profile of Mg^{3+} implantation at 180keV in GaN



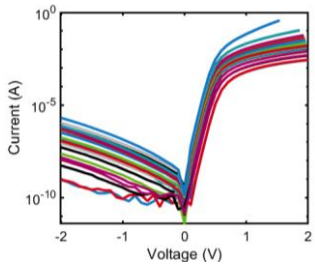
We started experiments on Mg-ion implantation for p-GaN. We use TEM, XRD, UV-VIS and IR measurements to evaluate the wafer damage after implantation. In addition, we completed the detailed design of a new MeV ion implanter tool and ordered all necessary tool parts.

Backside access and membrane processing

Microscope image of Schottky diode wafer backside through etched cavern



Schottky diode characteristic for different Schottky contact diameters



For vertical GaN-on-Si power devices, we were able to show promising results for membrane processing and handling using temporary bonding and debonding combined with local substrate and buffer removal. The transition from smaller wafers to 200 mm wafers is ongoing and for local substrate removal has taken place in production environment for the first time.

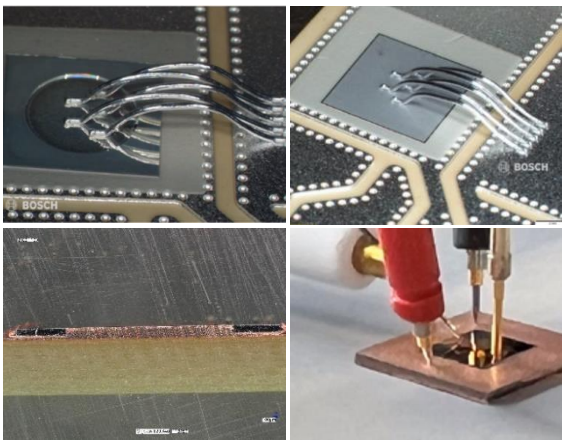
For all power devices contact formation is critical and therefore characterized to optimize the treatment of the contacts. To this end, we employ advanced lithographic structuring of transfer length method test structures on the backside of GaN membrane inside deep cavities to get information on the backside contacts only.

For the first time, we have processed vertical Schottky diodes on full 150 mm GaN-on-Si wafers. We achieved membrane diameters up to 4.5 mm without damage thanks to frontside protection by a temporarily bonded carrier. The diodes are rectifying thus showing that the membrane process developed in YESvGaN enables vertical current flow without affecting the electrical functionality.

Assembly and interconnection technology

The main challenge in assembling the vertical GaN devices is the connection of the thin membrane and the heat dissipation during operation. Thus, the membrane needs to be contacted without any voids. The topology and fragileness of the membrane chips demands for adapted or new developed interconnection technologies. We developed sintering and soldering solutions for the contact of the chips. We demonstrated the interconnection technologies with a functional GaN Schottky diode by measuring its characteristic before and after the joining process. Cross sections have shown, that the chips are connected well. Additional measurements have been performed to access the material data of the GaN stacks within the device. The next step is to join GaN diodes which will undergo several reliability tests afterwards.

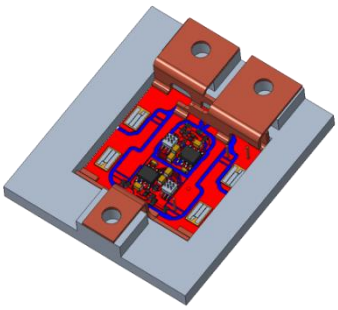
Interconnection technology used in YESvGaN



Application efficiency

In the second project year, we focused on the design and development of a halfbridge power module (HBPM) as application-oriented demonstrator of our vertical GaN transistor. The HBPM combines one concept and a multitude of possibilities. Two different packaging concepts have been implemented – first, transistors as bare die chips mounted on DCB for high thermal and electrical performance, and second, packaged discrete devices assembled on IMS for medium power and as low-cost solution. The module concept needs to be compatible with existing state of the art SiC transistors to evaluate the performance of the module design and also for the new vertical GaN transistors. As first step the HBPM has been set up with SiC devices. The outer dimensions for the DCB are 65 mm x 58 mm. The measurements and characterization of the HBPM are ongoing. The current version of the DCB concept with SiC devices will be presented on the PCIM fair in May 2023 in Nuremberg.

HBPM using SiC transistors assembled on DCB incl. frame



Closing words

As it was outlined in this newsletter, the work of the YESvGaN consortium during the last year has led to significant advances in all aspects of our technology development. As the new concept of vertical GaN membrane transistors is very complex, each design element needs to be optimized while having its impact on the remaining fabrication steps in mind. Therefore, it is a big asset that the consortium covers the whole semiconductor value chain and we strongly benefit from combining the expertise of all our partners from semiconductor processing over tool manufacturing and advanced characterization up to assembly and application.

After promising results in terms of blocking capability of the epitaxial stacks, conduction properties of the transistor channels, first demonstrations of fully vertical diodes and their assembly, we are eager to provide our first fully vertical transistors in the third and last project period. So, stay tuned and keep following us on our social media channels for latest updates!

Future events

April 16-19	Our partners are presenting at EuroSimE 2023 in Graz, Austria
May 9-11	Meet and greet our partners at the PCIM fair 2023 in Nuremberg, Germany
May 15-18	Watch the presentations of our partners at CSMANTECH 2023 in Orlando, Florida
August 28-30	Join our PhD summer school on GaN and SiC power electronics in Gent, Belgium

Popular press

The first 200 mm SOI dummy wafers are coming out of the production line! Temporary wafer bonding, grinding, backside lithography and cavity etching, resulting in a final membrane thickness of 5 µm plus 1 µm BOX thickness. We cannot wait to start with the GaN wafers! #XFAB #GaN #powerelectronics #YESvGaN

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