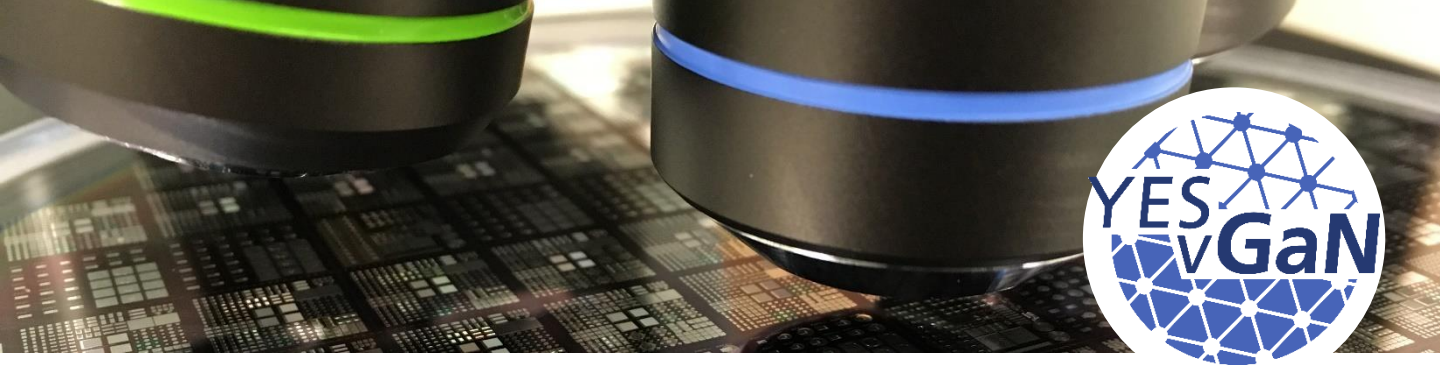


YESvGaN

Wide bandgap power at silicon cost

Newsletter 3 – June 2024

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 101007229. The JU receives support from the European Union's Horizon 2020 research & innovation program and Germany, France, Belgium, Austria, Sweden, Spain, Italy

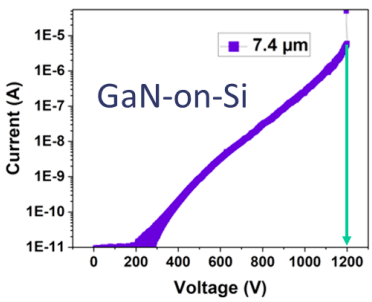
Introduction

An exciting third YESvGaN project year has come to an end. Over the past 12 months, our partners have made significant progress in epitaxy, processing, and application. We are delighted to report an increase in GaN drift layer thickness, resulting in a blocking voltage of up to 1200 V. Additionally, we have achieved full process integration on 200 mm GaN-on-silicon substrates, advancements in assembly and interconnection technology of membrane transistors, and the development of application demonstrators based on GaN-ready half-bridge power modules. Notably, we have successfully completed our first fully-vertical GaN-on-silicon Trench MOSFET demonstrator, showing the feasibility of vertical GaN membrane transistors on foreign substrates for future power transistors. Below you can find an excerpt of the highlights from our work packages.

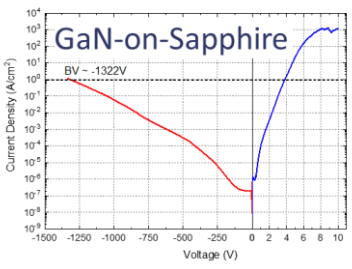
Development of vertical drift epitaxy

Epitaxy development covers a wide range of the supply chain, ranging from MOCVD equipment, to actual epitaxial growth and test devices, including characterization techniques during growth, after growth and after device manufacturing. Vertical drift layer stacks have been grown on Si and sapphire with a record-high diode breakdown of 1200 V on 150 mm Si and above 1300 V on sapphire. On both substrates, we were able to demonstrate avalanche breakdown behaviour.

Reverse I-V curves of pn-diodes on 150 mm Si with 1200 V breakdown voltage.

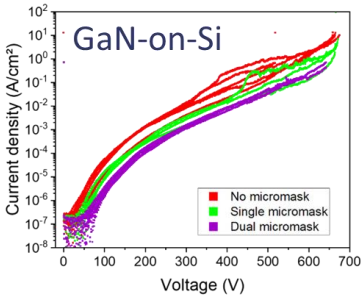


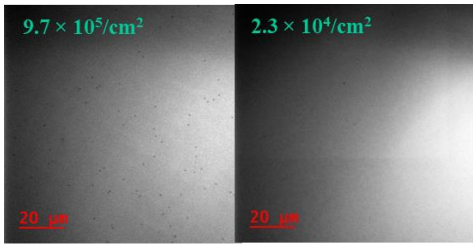
Electrical leakage was successfully reduced by incorporating a micromasking technique during the growth. Dislocation densities on Si went down to $1 \cdot 10^8$ cm^{-2} with further room for improvement. On the 300 mm MOCVD prototype system all critical layers for vertical device stacks have been tuned in with excellent uniformity.



Reverse I-V curves of pn-diodes on sapphire with above 1300 V breakdown voltage.

A comparison of dislocation density for GaN on native HVPE and ammonothermal substrates yielded threading dislocation densities in the range of $1 \cdot 10^6$ and $2 \cdot 10^4$ cm^{-2}, respectively, setting an ambitious lower target for heteroepitaxial GaN.





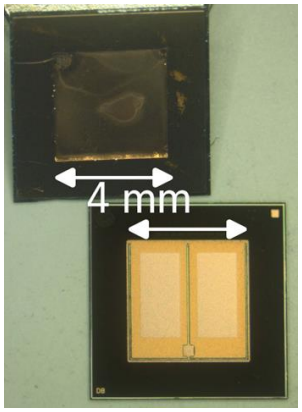
5 µm GaN on HVPE GaN

5 µm GaN on ammonothermal GaN

Left: Leakage current reduction by the application of micromasking layers that reduce the threading dislocation density. Etch pit density showed a dislocation density of about $1 \cdot 10^8$ cm^{-2} for the samples with dual micromask. Right: Cathodoluminescence micrographs of 5 µm GaN buffers on top of either HVPE GaN substrates or ammonothermal GaN substrates showing dislocation densities of ~$1 \cdot 10^6$ cm^{-2} and ~$2 \cdot 10^4$ cm^{-2}.

Development of vertical GaN power transistors

The first processed device wafers of fully vertical GaN-on-silicon MOSFETs



First fully vertical GaN-on-silicon membrane Trench MOSFET chips

The YESvGaN target transistor concepts, Planar Gate MOSFET, Trench Gate MOSFET and FinFET have been improved by the responsible partners in the last period. For Planar Gate MOSFETs, a full frontside process flow on 200 mm GaN-on-silicon wafers was demonstrated in a CMOS fab including an optimization of the source implant. This is an important step as it shows that it is possible to process these wafers in a state-of-the-art manufacturing environment despite the fragility of 200 mm GaN-on-silicon wafers with drift epitaxy.

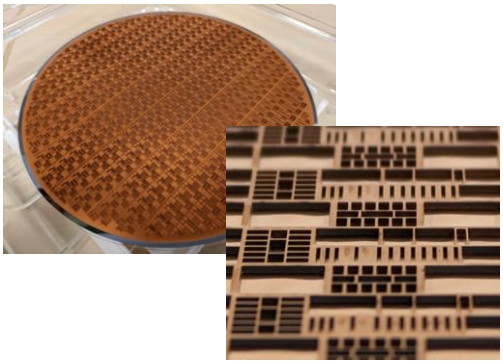
For Trench Gate MOSFETs, the gate module and its impact on transistor performance has been thoroughly characterized using advanced electrical characterization methods coupled with TCAD modelling. This showed that two types of traps, border traps and interface traps, are responsible for the hysteresis and sub-threshold swing in the transistors transfer characteristic, respectively. Process optimization allows the density of these traps to be reduced thus improving transistor performance. Finally, fully vertical Trench MOSFETs with relevant dimensions up to 16 mm^2 were demonstrated on 150 mm GaN-on-silicon wafers. They yielded a specific on-resistance of 6.3 $m\Omega.cm^2$. To the best of our knowledge, this is the first time that a fully vertical GaN-on-silicon transistor with such large area has been demonstrated and is an important step in showing the feasibility of the technology.

For FinFETs, it could be shown that the accumulation channel of the FinFET when paired with an advanced ALD gate dielectric behaves very favourably as it does not suffer from a reduced channel mobility at higher temperatures.

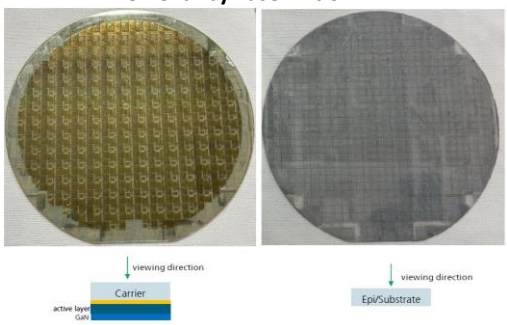
One of the major challenges in this work package is the development of a process for p-type implantation and activation. For the implantation part, a new implanter tool capable of high temperature Mg implantation for up to 200 mm wafers has been developed and is currently under assembly. For the activation, the consortium employs advanced methods such as pulsed rapid thermal annealing and uses optical techniques such as Raman spectroscopy and spectroscopic ellipsometry to assess recovery of the crystal damage and scanning measurements such as Kelvin probe force microscopy in addition to standard electrical characterization to get further insights into the polarity of the charge carriers.

Backside access and membrane processing

Complete processed 200 mm GaN-on-Si vertical device wafer with ohmic backside contacts



First successful sapphire growth substrate removal by laser lift off



Several 150 mm and 200 mm GaN-on-silicon wafers with fully vertical devices were successfully processed through the entire backside process chain, including temporary bonding, backside etching, metallization and debonding. This includes the first 200 mm device wafers which showed successful contacting from the backside with an ohmic contact characteristic. The first generation of fully vertical Trench MOSFETs on a 150 mm device wafer was fabricated and can now be used for assembly and interconnect technology tests.

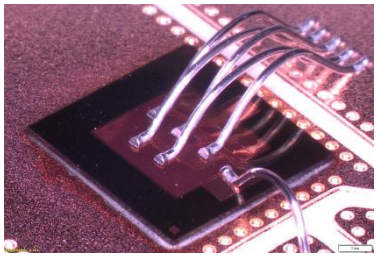
A critical part of power device manufacturing is the quality of the contacts. Within this project it was found that for the backside contact formation a chemical wet pre-treatment improved the ohmic behavior dramatically.

Besides the achievements in the field of GaN-on-silicon backside process technology, GaN-on-sapphire substrates were also considered in this project. For these substrates, the removal of the sapphire growth substrate enabling true vertical devices is crucial and was first achieved within the last year with laser lift off (LLO). A complete 100 mm GaN-on-sapphire device wafer was first temporarily bonded and then the growth substrate was removed by LLO.

Assembly and interconnection technology

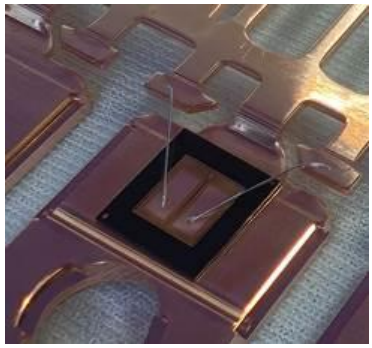
Within YESvGaN, we achieved our first successful bonding of vertical GaN diodes and transistors onto direct copper bonded (DCB) substrates.

The bonding was successfully carried out using soldering and nanowire sintering (KlettSintering) on specially prepared substrates. During soldering, copper plates were inserted into the chip cavities to minimize the deflection of the membrane. In KlettSintering, the substrates were structured in such a way that they represented the inverse of the chip geometry.



Vertical GaN chip soldered to a DCB and wire bond top interconnects

The top-side contacting was subsequently carried out using aluminium wire bonding. Test diodes withstood the assembly process well and were subsequently measured.



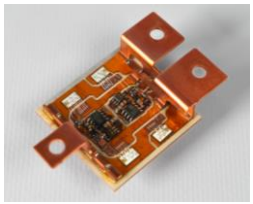
Vertical GaN diode chip mounted on a copper lead frame including wire bonding

These processes formed the basis for carrying out the assembly of the first vertical GaN transistors. A transistor contacted by the special developed soldering process and subsequent wire bonding was successfully measured. Transistors contacted on substrates were handed over to WP6. This will allow the project partners from the application work package to characterize these transistors using standard setups.

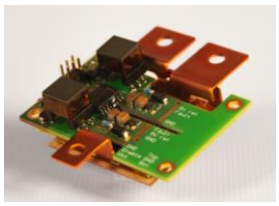
In addition to our current work, we will also fabricate discrete vertical GaN diodes by assembling diodes to lead frames and subsequently moulding them. Thereby, a better comparison to conventional semiconductors can be made.

Application efficiency

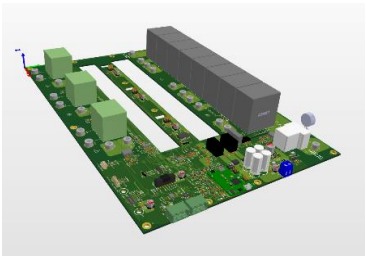
The vertical GaN-ready half-bridge power module (HBPM) combines one concept and a multitude of possibilities. Two different packaging concepts - bare die chips mounted on a DCB substrate and packaged discrete devices on an insulated metal substrate (IMS) - are developed and assembled. In a first step, the performance of the newly developed module will be examined and verified using state-of-the-art SiC MOSFETs.



Packaging concepts: bare die chips mounted on DCB for high thermal and electrical performance

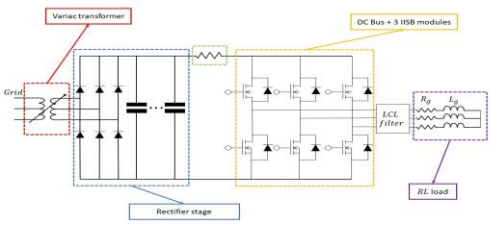


HBPM with adapter board for control and galvanic isolation



Rendering of the DC BUS Power Module

During the third year of the project, partner *Raw Power* designed the DC BUS PBC which mounts 3 HBPMs produced by partner *Fraunhofer IISB* and which will be part of the three-phase scaled PV demonstrator. The PCB is under production phase in partner *Aurel S.p.A.*'s facility, first tests will be held at the beginning of June at *Raw Power*.



Block diagram of the scaled PV demonstrator

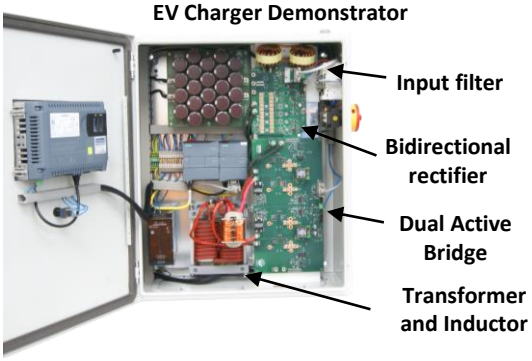
Tests will be performed in a dedicated area where the setup of the scaled PV demonstrator will be prepared. According to the block diagram of the PV demonstrator, the actual PV array will be replaced with a variac of 11 [kVA] and a rectified stage. The variac will also be useful to perform tests of HBPMs at different input voltage values. Initially, the load will be represented by an RL load coupled with a LCL filter. During the tests, the efficiency of the inverter mounting HBPMs will be monitored and analyzed.

Partner *SiCtech* has developed the application-oriented demonstrators. In the case of the induction heating application, a half-bridge inverter was developed. The inverter output is connected to a transformer which serves as a matching transformer. The resonant tank is a series LC consisting of a 2 μH inductor and a capacitor bank with a connection range of 0.33 μF to 1.98 μF. This allows working in a frequency range of 200 to 80 kHz. The final specifications of the demonstrator are 25 kW with a maximum output current of 127 Arms.

Induction Heating Demonstrator

The demonstrator for electric vehicle chargers integrates the dual active bridge (DAB) converter. The converter has a 1.66 ratio transformer on its outputs to operate with rectified single-phase voltage and a battery voltage range between 400 and 285 V. The transformer leakage inductance is complemented by a 10.5 μH inductor to enable smooth zero voltage switching (ZVS) switching over the entire operating range of the converter, and the operating frequency is 130 kHz. The charger is designed for bidirectional operation, meaning it can charge and discharge the battery of the electric vehicle. To enable this functionality, a single-phase bidirectional rectifier has been developed that functions as a boost rectifier for battery charging and as a sinusoidal pulse width modulation (SPWM) inverter for grid injection. The input filter consists of two 72 μH inductances and a 17.7 μF capacitor bank.

EV Charger Demonstrator



Summer school 2023

The YESvGaN-TRANSFORM-PowerElec summer school was a great success with 72 participants and 15 speakers, coming from academia and industry from all over Europe. All lectures - available on the YESvGaN YouTube channel - from basic power electronics to applications, were received with great enthusiasm and new friendships have been created during the social networking events. We want to thank you all for your participation. We hope to see you again in the future!

Closing words

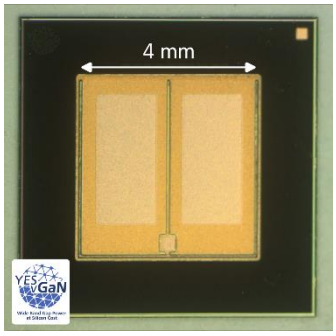
With the technical achievements of the third project year, we are nearing the finish line. We take pride in significantly advancing the field of vertical GaN transistors on foreign substrates. In addition to the successful demonstration of a fully-vertical GaN-on-silicon Trench MOSFET, we have gained valuable insights into the challenges that still need to be addressed in the future. These include further reducing reverse leakage current in the epitaxial layers, integrating area-selective p-type doping into GaN transistors for proper shielding, and reducing backside topography for improved assembly.

Before the conclusion of YESvGaN in October 2024, there is still ground to cover. Our final transistor lots need to be completed, and we must enhance our understanding of the behaviour and reliability aspects of the available transistors. Be sure to follow YESvGaN on the different social media platforms listed below to stay updated on important developments.

Future events

July 8-12	Learn all about GaN from our partners at the SSIE summer school in Brixen, Italy
September 15-27	Thermal characterization of vertical GaN at Therminic 2024, Toulouse, France
November 3-8	Meet and greet our partners at IWN 2024, O'ahu, Hawai'i

Popular press



Oops we did it … a GaN transistor!
YESvGaN proudly announces that the first fully vertical GaN-on-silicon Trench MOSFETs are finished. They demonstrate the feasibility of our vertical GaN membrane transistor concept for large active areas up to 16 mm^2. Be sure to attend this year's GaN Marathon to be the first to learn about the electrical results.

#galliumnitride #GaN #powerelectronics #mosfet #britneyspears

YESvGaN.eu @YESvGaN YESvGaN YESvGaN